REMARKS

Claims 3-42 and 58-64, as amended, remain herein.

Applicants appreciate the statements in the Office Action that claims 3-42 are allowed.

Claims 5, 7, 10, 12, 58, 60 and 61 have been amended to replace the phrase "capacities between parasitic gate lines" with "parasitic capacities between gate lines." Claims 1, 2, 43 and 44 have been cancelled without prejudice or disclaimer.

1. The finality of the restriction requirement is acknowledged.

2. Claims 1, 2, 43 and 44 were rejected under 35 U.S.C. §102(e) as anticipated by Nakamura et al. U.S. Patent 6,069,620. Claims 1, 2, 43 and 44 have been canceled, thereby mooting the rejection.

3. Claims 58-64 were rejected under 35 U.S.C. §103(a) over Nakamura et al. '620 in view of Nakamura et al. 6,005,646.

The presently claimed method is for driving a liquid crystal device to cause transition from a splay configuration to a bend configuration of a liquid crystal layer, located between a first substrate on which thin film transistors and pixel electrodes are located in a matrix and a second substrate on which an opposing electrode is located, the method including: continuously applying a potential difference, different from a potential difference in a normal image display period, between the pixel electrode on the first substrate and the opposing electrode on the second substrate, wherein, storage capacities connected to the pixel electrodes are formed between the pixel electrodes and common electrodes having potentials common to all the pixel electrodes, so that, by means of a ratio between pixel electrode capacities including the storage capacities and parasitic capacities between gate lines of the thin film transistors and the pixel electrodes, potential variation of the pixel electrodes accompanied by potential variation of the

common electrodes results in a potential difference. This method is nowhere disclosed or suggested in the cited reference.

The Examiner admits that Nakamura et al. '620 does not disclose storage capacities connected to the pixel electrodes as being formed between the pixel electrodes and common electrodes having potentials common to all the pixel electrodes, and cites Nakamura et al. '646 as allegedly teaching a liquid crystal display device and its equivalent circuit having the following features.

Nakamura et al. '646, column 4, lines 1-16 and Fig. 7 discloses drain electrode in TFT 6 connected to a gate line 20, which is connected to gate line driving circuit 16. A source electrode in TFT 6 is connected to a display electrode. Liquid crystal material is located between the display electrode on an array substrate and common electrode 22 (corresponding to applicants' opposing electrode) on an opposing substrate. This liquid crystal constitutes a liquid crystal capacity 8. Common electrode 22 is driven by common electrode driving circuit 24. A portion of each display electrode (corresponding to applicants' pixel electrode) is located above front gate line 20

to constitute auxiliary capacity 10 (corresponding to applicants' storage capacity). Parasitic capacity 12 is located between the gate and source in TFT 6.

In contrast, applicants' method for driving a liquid crystal device recited in claims 58 and 60 is based on the concept that potential variation is provided to the common electrode, which constitutes a storage capacity with the pixel electrode, and that potential variation is used with the potential variation of the pixel electrode. Nakamura et al. '646 does not disclose or suggest a method wherein storage capacities connected to the pixel electrodes are formed between the pixel electrodes and common electrodes having potentials common to all the pixel electrodes, so that, by means of a ratio between pixel electrode capacities including the storage capacities and parasitic capacities between gate lines of the thin film transistors and the pixel electrodes, potential variation of the pixel electrodes accompanied by potential variation of the common electrodes results in a potential difference, as recited in applicants' claims 58 and 60.

Applicants' claims 59 and 61 are based on the concept that potential variation is provided to the gate line one line front or behind, which constitutes the storage capacity with the pixel electrode, and that potential variation is used with the potential variation of the pixel electrode. Nakamura et al. '646 does not disclose or suggest a method wherein storage capacities connected to the pixel electrodes are formed between the pixel electrodes and the gate lines one line front or behind, so that, by means of a ratio between pixel electrode capacities including the storage capacities and capacities between parasitic gate lines of the thin-film transistors and the pixel electrodes, potential variation of the pixel electrodes accompanied by potential variation of the gate lines one line front or behind results in the potential difference, as recited in applicants' claims 59 and 61.

A comparison between Nakamura '646, column 4, lines 1-16 and Fig. 7, and applicants' claims 58-60, shows that Nakamura '646 discloses only a front gate line located opposed to a pixel electrode and forming an auxiliary capacity between the gate line and the pixel electrode, and that Nakamura '646 does not

disclose or suggest anything about the features recited in applicants' claims 58-61.

For the foregoing reasons, neither Nakamura '620 nor Nakamura '646 contains any teaching, suggestion, reason, motivation or incentive that would have led one of ordinary skill in the art to applicants' claimed invention. Nor is there any disclosure or teaching in either of these references that would have suggested the desirability of combining any portions thereof effectively to anticipate or suggest applicants' presently claimed invention. Claims 62-64, which depend from claims 58-60, respectively, are allowable for the same reasons explained herein for claims 58-60. Accordingly, reconsideration and withdrawal of this rejection are respectfully requested.

All claims 3-42 and 58-64 are now proper in form and patentably distinguished over all grounds of rejection stated in the Office Action. Accordingly, allowance of all claims 3-42 and 58-64 is respectfully requested.

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Should the Examiner deem that any further action by the applicants would be desirable to place this application in even better condition for issue, the Examiner is requested to telephone applicants' undersigned representatives.

Respectfully submitted,

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